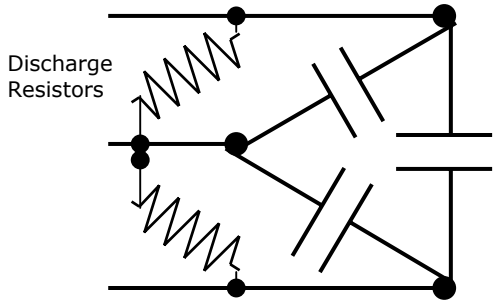
Technical Note
Discharge devices for high speed dynamic switching.

Standard Discharge Resistors:
Normally the capacitor manufacturer as a part of their normal supply provides discharge resistors across the capacitor banks. This is mainly to cater for the human safety requirements, which are mandatory, part as per IEC, IS or any other internationally known standards for the Power Factor improvement capacitors.

Normally, the resistors put are of a very high value and the value is adjusted such that peak voltage across the capacitors should be less than 48Volts (depends on standards) in less than a minute of disconnecting the capacitors from mains.



The diagram shown above depicts the typical positioning of the standard discharge resistors.

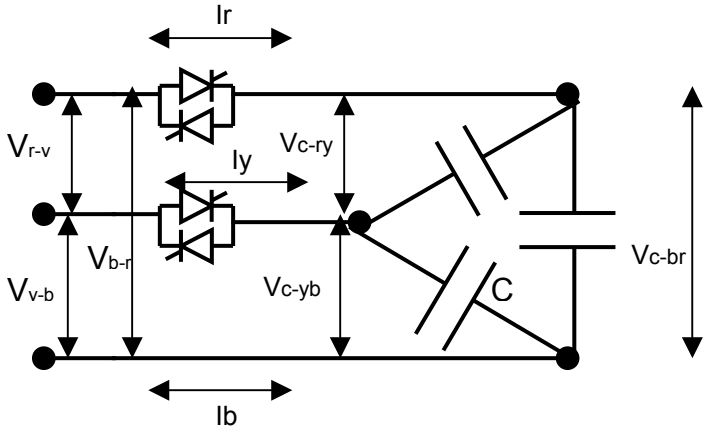
What is the situation with high-speed dynamic response:
We need to analyse the situation with two different thyristor switching configurations because the different configurations put different selection criteria for the discharge device selection. Viz.:

1. Two thyristor configuration in Line: (or same as three thyristors in Line)
2. Thyristor blocks within the delta arms of capacitors.

The situations can be understood from some initial explanation as given below.

Conditions for switch OFF with 2 thyristor in line configuration:

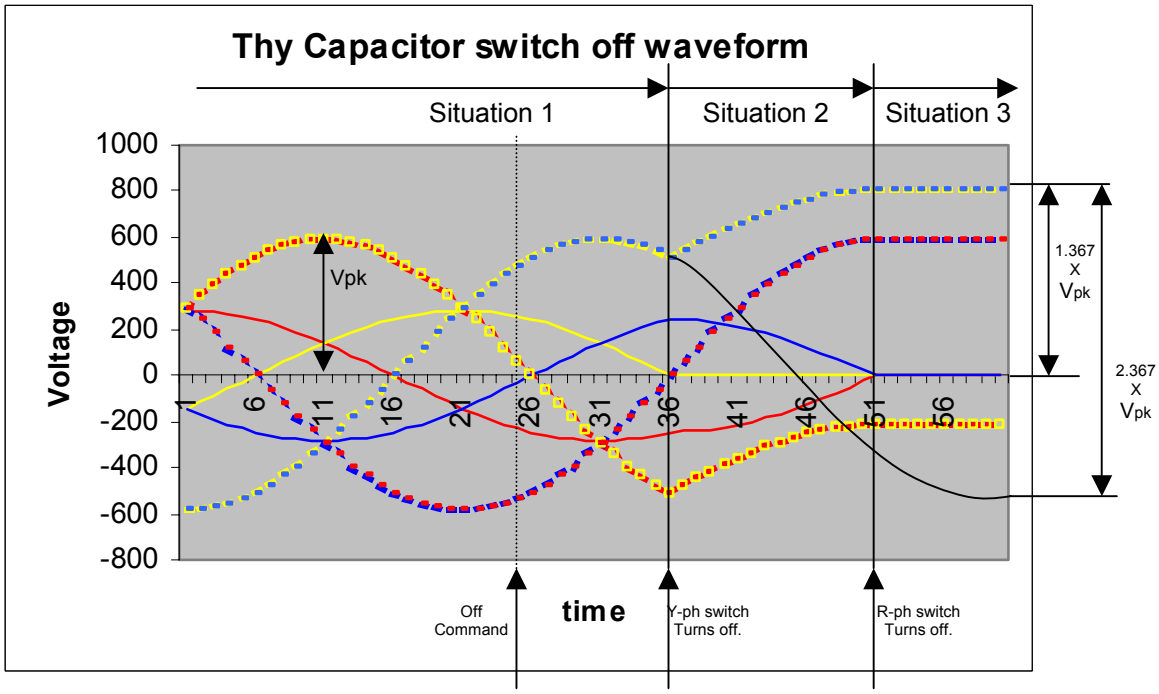
Consider the following diagram. This shows the various Line Voltage Waveforms and the Current waveforms passing through the thyristor switches.



The diagram shown above is for the waveform “Situation 1” where both the R-ph and Y-ph thyristor switches are conducting.

Ir	———	Vc-ry	·····
Iy	———	Vc-yb	·····
Ib	———	Vc-br	·····

Vpk = Peak of Line voltage.

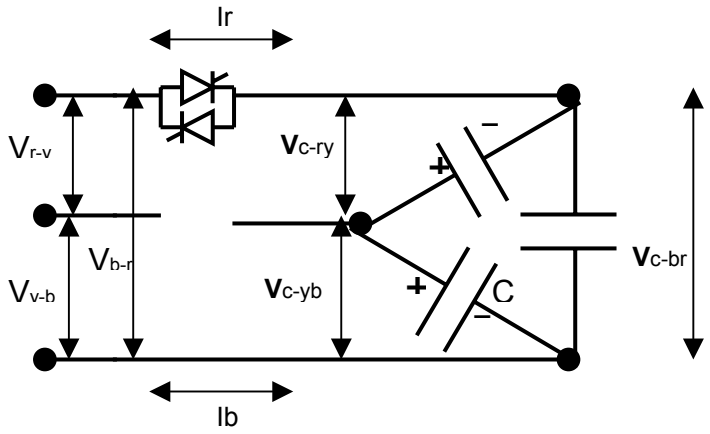


Now view what happens in Situation 1.
The turn Off command from the PF controlling relay is given at any random instance. This will immediately turn off the gate driving to the thyristors.

But thyristors being current sensitive elements, does not turn Off immediately. Thyristors can only turn off by its natural commutation at zero instant of current waveform.

In the thyristor switches (thyristors in 2 phase only) we have assumed that B-phase is the direct phase and current through it can only be off if both the thyristors in other two phases is Off.

In the above waveform situation, the first zero current is experienced by Y-phase thyristor block. Under this condition, the Y phase thyristor is switched Off and the effective diagram that can be seen (going from Situation 1 to Situation 2) is as given below.



Under this situation, **at the instant of Y phase thyristor turn-Off**, we can see following points.

- Vc-ry = Vc-yb = Vpk √3 / 2 and with the polarity as shown in the diagram.
- Vc-br = 0.
- Capacitor across R-Y phase and capacitor across Y-B phase are seen in series.

Now in situation 2, only R phase thyristor is conducting,
Thus, Ir current would be only due to effect of Vb-r and load being only capacitive, this current would be 90° leading the Vb-r waveform. Thus, waveform current Ir and Ib (phase opposition to Ir) are getting phase shifted accordingly. This can be seen from the waveform.

Along the situation 2, Vc-br increases from 0 to Vpk (sine wave path). This also is the voltage across the series capacitor across R-Y and Y-B phase. As these capacitors are of equal value, this incremental voltage would be divided equally between these two capacitors. Thus, effective voltage across each capacitor would be (Vc-br/2) + (Vpk√3/2) with effective signs.

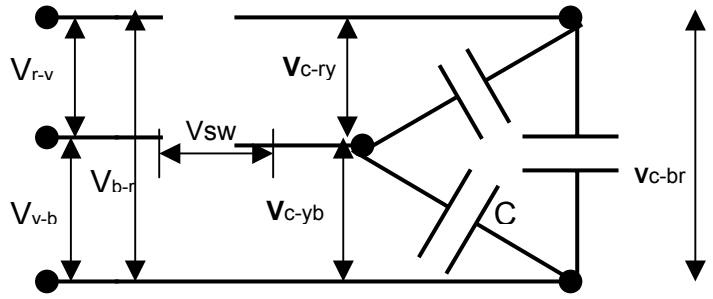
Thus in the given situation, capacitor across R-Y being charged negative, it will discharge and capacitor across Y-B being charged positive, will charge more.

When Vc-br is at its peak, the current Ir through R phase thyristor comes to its zero crossing instant. Under this condition it turns off.

At this instant Voltage across capacitors would be
Vc-ry = (Vpk/2) – (Vpk√3/2) = -0.367 Vpk.
Vc-yb = (Vpk/2) – (Vpk√3/2) = 1.367 Vpk.
Vc-br = Vpk.

Same values in terms of Line voltage values can be seen as (where V_{LINE} = Vpk/√2)
Vc-ry = -0.519 V_{LINE}.
Vc-yb = 1.933 V_{LINE}.
Vc-br = 1.414 V_{LINE}.

The diagram after the change-over from Situation 2 to Situation 3 can be seen as below.

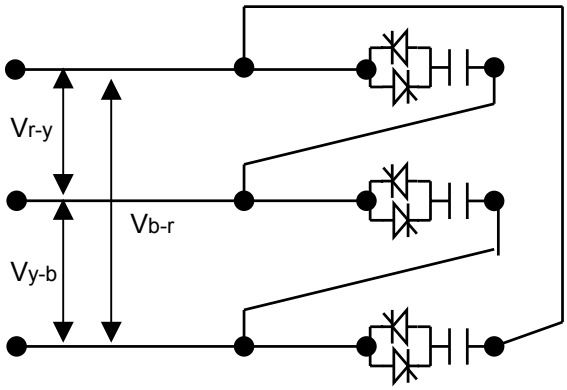


Now Vsw shown in this diagram is the voltage that can come across the off state thyristor switch. And from the waveform it can be seen that maximum voltage that can be seen by the blocked thyristor switch is with Y phase thyristor.

From waveform it can be seen that maximum blocking voltage for this thyristor required would be:
Vsw = 1.367 Vpk + Vpk = 2.367 Vpk
In terms of line voltage values, it is
Vsw = 3.348 V_{LINE}.

<u>Conditions for switch OFF for three thyristors in Delta arm configuration:</u>

The delta arm configuration diagram is as shown below.

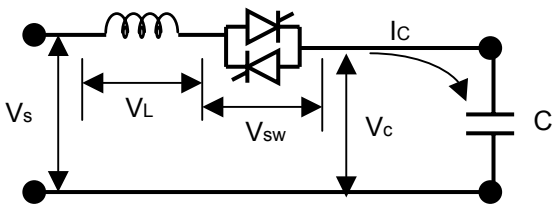


In this condition, the thyristors are seen within the delta arms. The capacitors to be used here are single cell capacitors.
But under this condition, individual capacitor cell is controlled by the thyristor. Under this condition, the thyristor turn OFF is at current zero so the 90° phase shift of voltage with respect to current keeps the **capacitors charged to maximum Vpk DC value** and the **maximum blocking voltage** experienced by the thyristor switches would be **2 Vpk**.

Lets even consider the conditions with addition of detuned reactor in the circuit:

If the detuned reactors are added, the voltage across the capacitor proportionately increases equivalent to the reactor voltage drops.

To understand this phenomenon, consider the following situation where to understand the subject better, we have consider the single phase supply condition.



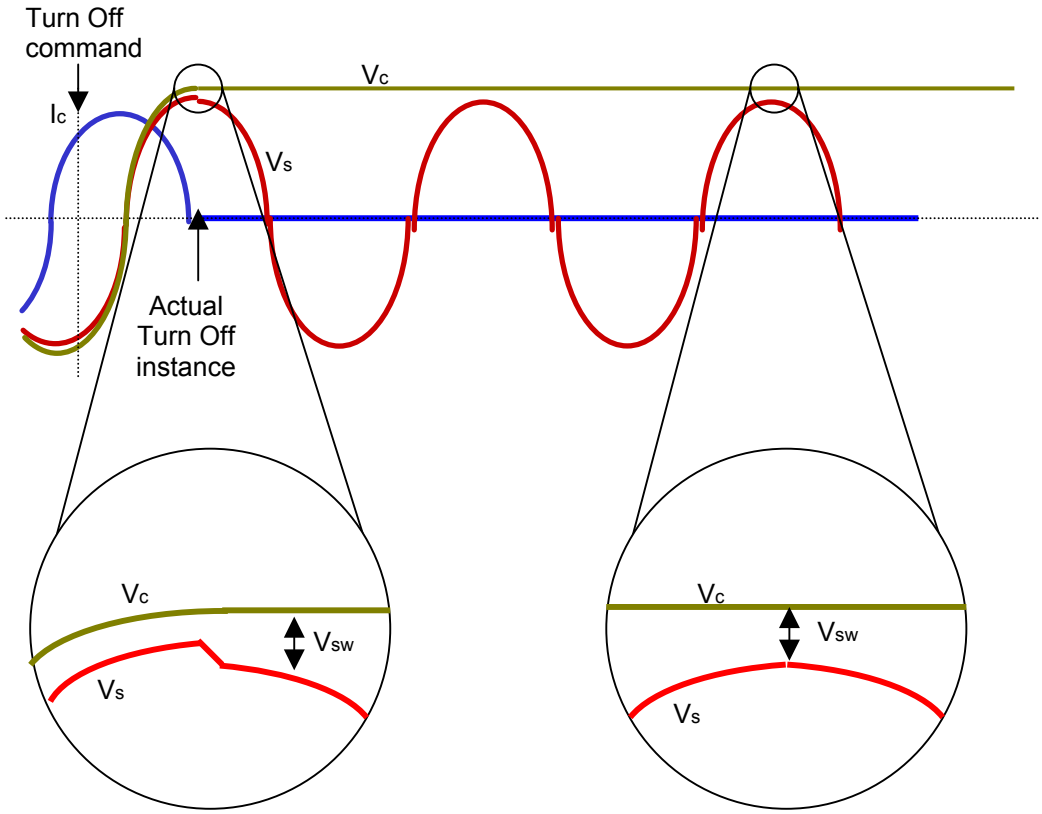
Here
Vs is the voltage applied.
Vc is the voltage across the capacitor with capacitance value as 'C' in Farads.
Ic is the current flowing through the capacitor.
Vsw is the voltage across thyristor switch.
VL is the voltage across series reactors.
The phasor representation after neglecting Vsw shows the Vc value more than Vs.

Turn Off Situation:

Following waveform shows the exact voltage and current situations at the instant of turn off.

Note some technical considerations before analyzing the waveform

- Thyristors turn off only at current zero.
- As capacitor current leads voltage across it by 90°, at current zero, voltage across the capacitor is at its peak value.
- The voltage across the capacitor is higher than the mains voltage due to series reactors. Voltage across the series reactors (vector summation) added to mains voltage gives the capacitor voltage.
- When capacitors are removed from the mains circuit, the mains supply voltage tends to dip by small amount due to the source impedances.



From the diagram shown here, it can be seen that voltage across the thyristor switch never touches zero voltage level.

The discharge resistors across the capacitors that are provided by the capacitor manufacturer are of high value and thus for few tens of mains cycles (typically for 2 to 4 sec), the voltage across the thyristor switch is never touching zero mark.

For 415Vac line voltage (V_{LINE}) system with and with 7% line reactors (detuned), the typical value of minimum V_{sw} value observed with the turned off thyristor with maximum charged capacitor is:

1. For 2 thyristor in line configuration = 232Volts DC (can be derived from earlier explanation given for voltages)
2. For 3 thyristors in Delta arms configuration = 45Volts DC.

<u>Following chart shows minimum and maximum Vsw values as well as maximum DC voltage across capacitor: (Values given in terms of Line to Line voltage values)</u>

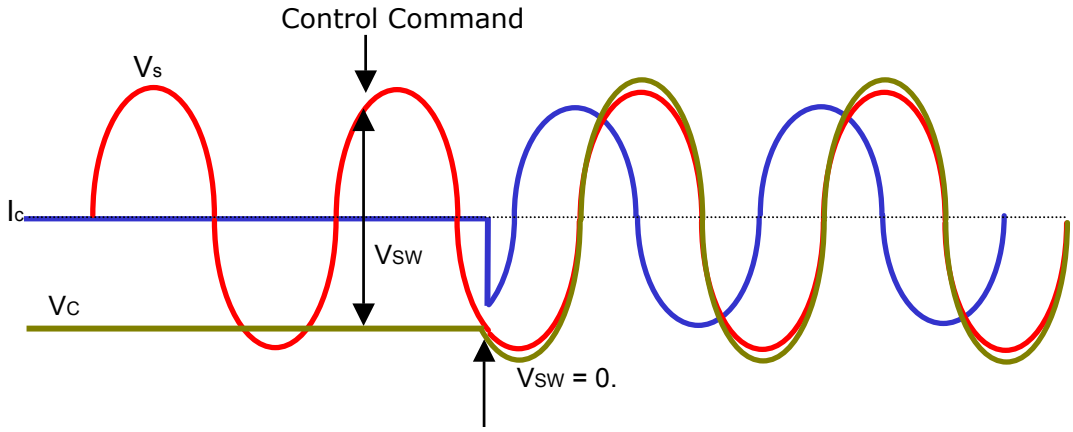
Sr.	Configuration	Vsw-Min	Vsw-Max	Vc-Max dc
1	Thyristors in 2 phases in line without Detuned reactors.	0.52 V_{LINE}	3.35 V_{LINE}	1.93 V_{LINE}
2	Thyristors in 2 phases in line with Detuned reactors 7.56%	0.56 V_{LINE}	3.58 V_{LINE}	2.07 V_{LINE}
3	Thyristors in 3phase inside Delta arms without reactors.	0	2.83 V_{LINE}	1.41 V_{LINE}
4	Thyristors in 3 phase inside Delta arms with reactors 7.56%	0.11 V_{LINE}	2.94 V_{LINE}	1.52 V_{LINE}

Minimum values are useful for calculating response time as can be seen from following discussions.
The maximum values are useful for calculation of worse case blocking voltages that can appear across the OFF thyristor block.

Turn On Situation:

Here is the typical turn-on situation waveform.
Note the following technical point before analyzing the waveform:

- Capacitor switch-on by thyristor switches is when the differential voltage (V_{sw}) across the thyristor switches is very near zero. With TAS make ZCCP or ZCTC thyristor switches; this value is typically ±3Volt dc.



From the diagram above, it is seen that thyristor switches waits after the control command, till it observes the value of Vsw = zero.
The moment it observes the value to be zero after that, it turns on the thyristor at that instant. Practically, this instant is within the tolerance of 2 to 3μSec.
But if after the control command, if Vsw is never found near zero, the thyristor switch will never turn On the thyristors. This type of situation can be seen when the thyristor switches are turned Off and On very fast.

Lets analyse this situation of Thyristor turn off and then immediately turn on.

Turn Off and immediate Turn On situation:

This is a situation arising for the highly fluctuating loading conditions. For this the dynamic response of the system required is very fast.

Lets see the situation with Switch Off and Switch On within 2 mains cycles.

The value of the Vsw will vary depending on the configuration and usage of detuned reactors. This can be arrived at from the above given chart.

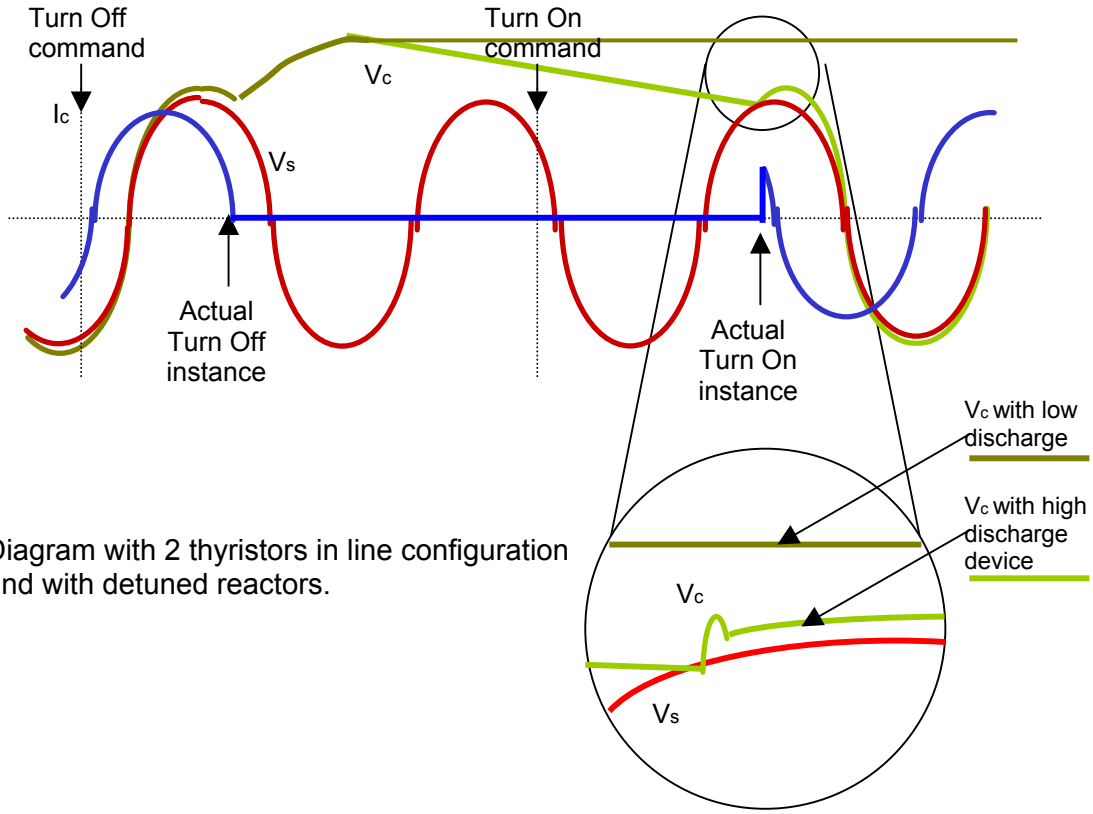


Diagram with 2 thyristors in line configuration and with detuned reactors.

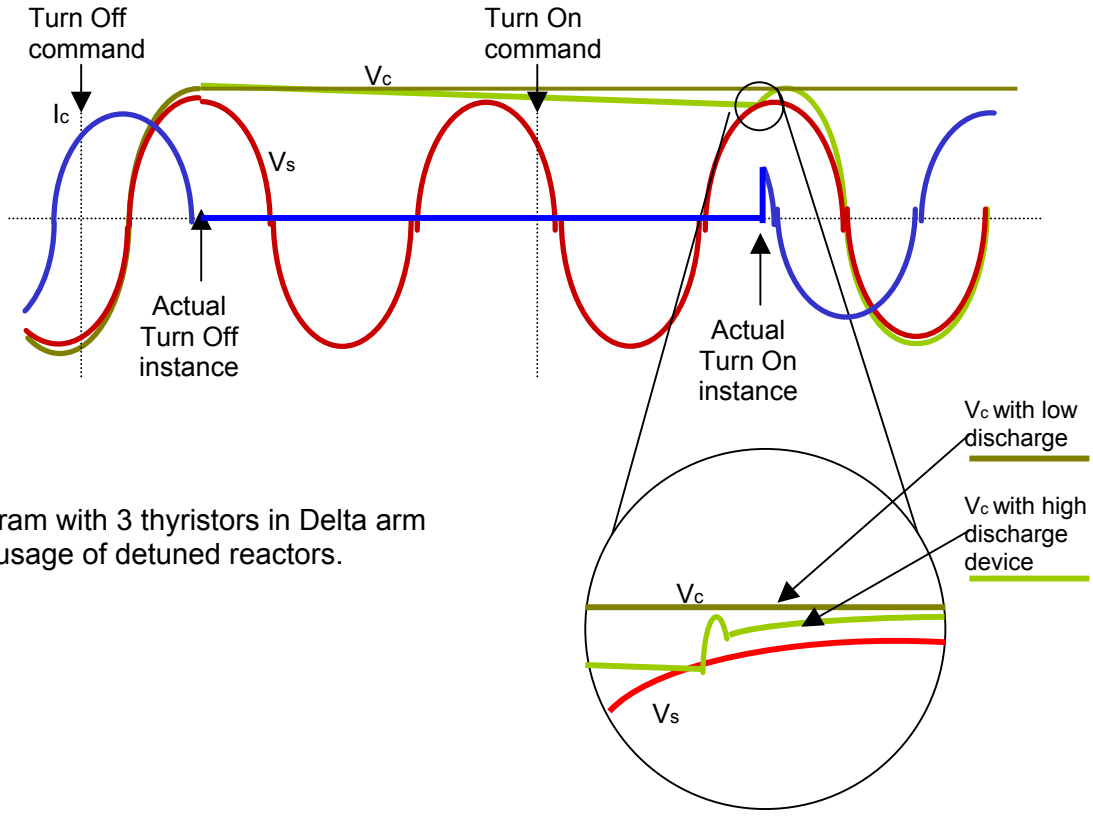


Diagram with 3 thyristors in Delta arm and usage of detuned reactors.

This diagram shows that if the capacitor is not discharged sufficiently so as to get V_{sw} to be zero, then even after the turn On command, the thyristor unit would not be switching On the capacitor banks within one mains cycle.
The diagram also explains the situation if a higher discharge devices are put across the capacitors. Under this case $V_{sw} = 0$ is achieved and switch turn-on is immediately within one cycle.

It can also be observed that the discharge devices that are required to be put with 2 thyristor in line configuration should be for much faster discharge. This is because of the capacitor voltage rise above the mains peak value almost by 35%.

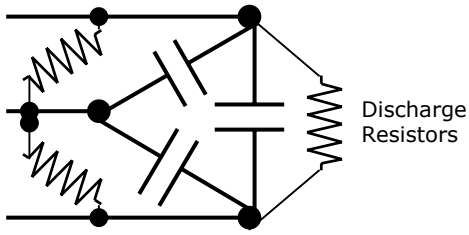
What Kind of Discharge Device is required:

The discharge devices are selected depending on the following criteria.

- Fastest dynamic response time required out of the system.
- Permissible watt-loss in discharge devices.
- Cost of discharge devices.

Discharge resistors:

The discharge resistors if used are put as shown in the diagram below.



The value of the discharge resistors would depend on fastest dynamic On – Off – On time requirement.
If “C” is the capacitor value in Farad,
“R” is the resistor value in Ohm.
“V_p” is the peak voltage (DC) across capacitor.
“ΔV” is the voltage reduction required in a minimum Off to On response time.
“τ” is the minimum Off to On time expected from system.

Then value of “R” in ohms (Ω) can be determined by formula:

$R = \tau / [C \{\ln (V_p/\Delta V)\}]$.

“ln” is Log of the term to base “e”.

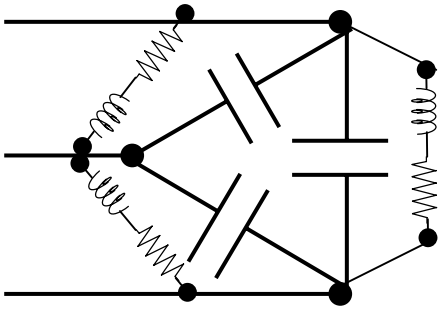
Pros and Cons:

- Discharge device prices are low.
- Can get good dynamic response.
- Capacitor On state watt loss is quite high and faster the dynamic response required, more is the watt loss expected.

TAS has a product called as “DISR-nn” that gives these discharge resistor modules for thyristorised capacitor switching application.
As ΔV value with 3 thyristors in delta arm configuration is low, automatically the value of R becomes higher and thus the watt loss in it reduces. Therefore for a very fast response time requirements with the thyristorised system, it is recommended to go with this type of thyristor configuration rather than 2 thyristor in line configuration.

Discharge Inductor + Resistor:

The diagram shows that the connections of discharge resistors and the inductors that are put across the Delta connected capacitors.



Here the value of inductor is selected such that it offers a very high impedance path for supply frequency “f” but has a very low value of resistance.
Resistance “R” is normally calculated as defined earlier.

Pros and Cons:

- Discharge device prices are much higher.
- Can get good dynamic response time.
- On state watt losses are minimized.

TAS has DISI-*nn* which is Discharge inductor + resistor combination for the said requirement.

END.